

	Add	Sub	LW	SW	BEQ (Taken)	Addi
<b>RegDst</b>	1	1	0	D	D	0
<b>ALUSrc</b>	0	0	1	1	0	1
<b>MemToReg</b>	0	0	1	D	D	0
<b>RegWrite</b>	1	1	1	0	0	1
<b>PCSrc</b>	0	0	0	0	1	0
<b>MemWrite</b>	0	0	0	1	0	0
<b>MemRead</b>	0	0	1	0	0	0
<b>ALUCtrl</b>	Add	Sub	Add	Add	Sub	Add

Note the don't cares (D) placed in the above table. Although **MemRead** can be a don't care for the SW instruction because the input to the address port is a legitimate address and will not raise an illegal address exception, the Data Memory unit cannot operate with both **MemRead** and **MemWrite** asserted. For a SW instruction, it is imperative that **MemWrite** be asserted (to 1) and therefore, **MemRead** must be a zero.

Also note that with the choices for the multiplexor variables in Fig. 5.17, the control signals **MemRead** and **MemToReg** are identical except for SW and BEQ for which MemToReg is a don't care (D). Hence the **MemToReg** control signal can be eliminated and the **MemRead** signal can be used in its place for this subset of instructions.