

COM S 321 Introduction to Computer Architecture and Machine-Level Programming
Fall 2009

Lectures: MWF 10 – 10:50 a.m., Gilman 0312

Recitations: Tuesday 9:00 – 9:50 a.m. in Pearson 108
Thursday 1:10 – 2 p.m. in Pearson 108

In addition, a lab exam will be conducted during recitation in Pearson 108. Other labs will also be held in Pearson 108.

NO RECITATIONS DURING THE FIRST WEEK OF CLASSES

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Prerequisites: Com S 228, CprE 281, Engl 250

Graded Course Work: Will consist of homework, frequent in-class activities, quizzes, and three exams. Weights for these will be provided later.

Office Hours: Mon, Fri, 9 – 9:50 a.m.

General approach: Concepts in computer architecture and machine-level programming will be explained as much as possible through solutions of problems in lectures, through in-class activities, and homework. It is a good idea for you to regularly attend lecture.

Students with Disabilities: Iowa State University complies with the American with Disabilities Act and Section 504 of the Rehabilitation Act. Any student who may require an accommodation under such provisions should contact me as soon as possible and no later than the end of the first week of class or as soon as you become aware. You will need to provide documentation of your disability to the Disability Resources (DR) office, located on the main floor of the Student Services Building, Room 1076, 515-294-6624. Please request that a Disability Resources staff send a SAAR form verifying your disability and specifying the accommodation you will need.

Course Objectives: To understand aspects of computer architecture and program performance. To adopt an evolutionary approach to learning by presenting fundamental concepts first in the context of an easy-to-understand instruction set such as MIPS, and building more complex ideas from the simpler ones.

Learning outcomes: Students will learn about computer performance, computer design, and tradeoffs between cost and performance as well as between hardware and software. Students will formulate and solve problems, understand the performance requirements of systems, and communicate effectively and learn to think creatively and critically, both independently and with others.

Outcomes: B, C, H

<http://www.cs.iastate.edu/gradadm/cmarquar/Undergraduate-Program-Outcomes.pdf>

Topical Outline

- 1. Introduction:** Computer abstractions and technology
- 2. Measuring and evaluating performance:** Metrics of performance; Amdahl's Law; Cost/benefit tradeoffs; Instruction count, CPI, Clock cycle time; Comparing and summarizing performance
- 3. Instruction set architecture of MIPS:** Signed and unsigned numbers; Representing instructions - the MIPS instruction set; Instructions for decision making; Supporting procedures - stack pointer; Arithmetic and Logical operations
- 4. Processor Datapath and control:** Building a datapath for R-type, I-type, and Jump instructions; A single cycle implementation; How control is supposed to work; A multicycle implementation and control
- 5. Memory Hierarchy design:** A framework for memory hierarchies; The basics of caches; Placement, replacement, and memory interaction policies; Measuring and improving cache performance; FIFO, LRU, write back and write through policies
- 6. Enhancing performance with pipelining:** Overview of pipelining; A pipelined datapath; Data hazards and forwarding; Data hazards and stalls; Branch hazards
- 7. Exceptions and exception handling:** Interrupts and exceptions; Hardware/software interface; Interrupt handlers

Textbook

Computer Organization and Design: The Hardware/Software Interface by Patterson and Hennessy, Second Edition.